

PATENT

2121  
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BT  
4-26-02

In re Application of:

: Atty. Docket No.: 00-LM-134

William A. CHREN, Jr.

: Group Art Unit: 2121

Serial No.: 10/033,992

: Confirmation No.: 9153

Filed: December 27, 2001

For: SELF-TIMED DIGITAL PROCESSING  
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INFORMATION DISCLOSURE STATEMENT

Technology Center 2100

Commissioner for Patents  
Washington, D. C. 20231

Sir:

The attached Form PTO-1449 provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that the information provided is prior art.

This IDS is submitted under:

- ☒ XX 37 CFR 1.97(b) - No Fee.  
☐ 37 CFR 1.97(c) - No Fee, with Certification.  
☐ 37 CFR 1.97(c) - Fee.  
☐ 37 CFR 1.97(d) - Fee, Certification & Petition.

The Commissioner is authorized to charge any required fees under 37 CFR 1.17(p) and (i) (1) to Deposit Account No. 50-1556.

Respectfully submitted,

Date:

4/15/02

By:

Stephen Bongini  
Registration No. 40,917

FLEIT, KAIN, GIBBONS,  
GUTMAN & BONGINI P.L.  
One Boca Commerce Center  
551 NW 77th Street, Suite 111  
Boca Raton, Florida 33487-1330  
Telephone: (561) 989-9811  
Facsimile : (561) 989-9812

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Form PTO-1449 U.S. Dept. of Commerce  
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**List of Documents**  
Cited by Applicant  
(Use several sheets if necessary)

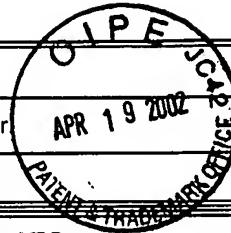
Atty. Docket: 00-LM-134

Serial No. 10/033,992

Applicant: William A. CHREN, Jr.

Filing Date: December 27, 2001

Group: 2121

**U.S. PATENT DOCUMENTS**

Ex'ts In'l		Document Number	Date	Name	Class	Sub- class	Filing Date, if applicable
	AA1	5,892,632	April 6, 1999	Behrens et al.			
	AA2	09/383,478					August 26, 1999
	AA3	09/656,550					September 6, 2000

**RECEIVED****APR 23 2002****FOREIGN PATENT DOCUMENTS** Technology Center 2100

		Document Number	Date	Country	Class	Sub- class	Trans'n Yes/No

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

	AA4	Chren, W.A. Jr., "One-Hot Residue Coding for Low Delay-Power Product CMOS Design", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, v. 45, no. 3, March 1998, pgs. 303-313.
	AA5	Karim Arabi et al., "Oscillation Built-In Self-Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits", Proceedings of the IEEE International Test Conference, Washington, D.C., 1997, pp. 786-795.
	AA6	N. S. Szabo, et al., "Residue Arithmetic and its Applications to Computer Technology, McGraw-Hill, 1967, pgs. 147-150.
	AA7	Chren, W.A. Jr., "A New Residue Number System Division Algorithm", Computers and Mathematics with Applications, vol. 19, no. 7, 1990, pgs. 13-29, 1990.
	AA8	Gago, A. et al. "Reduced Implementation of D-Type DET Flip-Flops", IEEE Journal of Solid-State Circuits, Vol. 28, No. 3, March 1993, pp. 400-402.
	AA9	Farrahi, A. et al. "Activity-Driven Clock Design", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 6, June 2001, pp. 705-714.
	AB1	Rabaey, J.M. "Digital Integrated Circuits: A Design Perspective", Prentice Hall, 1996, pp. 528-530.

Examiner:

Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.